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REMARKS

Reconsideration is requested in view of the above amendments and the following remarks. Claim 20 has been revised. Support for the revisions can be found at page 9, lines 17 to 28 of the specification, among other places. New claims 21-23 have been added. New claim 21 tracks previous claim 17; new claim 22 tracks previous claim 18; new claim 23 tracks original claim 19. Claims 7-14 and 16-19 have been canceled without prejudice. Claims 20-23 are pending in the application.

Claim Rejections – 35 USC § 103

Claims 7-10 and 12 are rejected under 35 USC 103(a) as being unpatentable over Bai et al. (US 2004/0222412) in view of Shim et al. (Moonsub Shim et al., "Polymer Functionalization for Air-Stable n-Type Carbon Nanotube Field-effect Transistors," J. Am. Chem. Soe. 123, pp. 11512-13 (2001)), and further in view of Takenaka (US 6,882,016). Claims 7 -10 and 12 have been canceled without prejudice, rendering the rejection moot. Applicants are not conceding the correctness of the rejection.

Claims 11 and 13-15 are rejected under 35 USC 103(a) as being unpatentable over Bai et al. in view of Shim et al., further in view of Takenaka as applied to claim 7, and further in view of Sato et al. (US 6,002,462). Claims 11 and 13-15 have been canceled without prejudice, rendering the rejection moot. Applicants are not conceding the correctness of the rejection.

Claims 16-20 are rejected under 35 USC 103(a) as being unpatentable over Dodabalapur et al. (US 6,278,127) in view of Shim et al., and further in view of Bai et al. Applicants respectfully traverse this rejection. Claims 16-19 have been canceled without prejudice, rendering the rejection moot. Applicants are not conceding the correctness of the rejection.

Claim 20 is directed to a method for manufacturing an electrical element array including an n-type field effect transistor and a p-type field effect transistor on a substrate. Claim 20 requires 1) forming a p-type semiconductor layer comprising carbon

nanotube between a source electrode and a drain electrode so as to form a plurality of p-type field effect transistors on a substrate, and then 2) forming an n-type modifying polymer layer only on the p-type semiconductor layer of a p-type field effect transistor that is included in the plural p-type field effect transistors and that should be converted into an n-type field effect transistor. The present method provides a simple process for manufacturing an electrical element array including p-type and n-type carbon nanotube field effect transistors on the same substrate (See page 4, lines 15-19 of the present specification).

The reference disclosures fail to teach or suggest the following steps in the order of 1) forming a p-type semiconductor layer comprising carbon nanotube between a source electrode and a drain electrode so as to form a plurality of p-type field effect transistors on a substrate, and then 2) forming an n-type modifying polymer layer only on the p-type semiconductor layer of a p-type field effect transistor that is included in the plural p-type field effect transistors and that should be converted into an n-type field effect transistor, as required by claim 20.

The rejection relies on Fig. 2 of Dodabalapur et al. as suggesting forming a p-type semiconductor layer between the source electrode and the drain electrode as required by claim 20. Applicants respectfully disagree. Fig. 2 of Dodabalapur et al. illustrates forming a metal-insulator-semiconductor field effect transistor (MIS-FET) type device including a p-n junction formed by a semiconductor layer 21 on top of another semiconductor layer 16 that is of the opposite conductivity. Nothing in Fig. 2 of Dodabalapur et al. teaches or even suggests that the semiconductor layer 21 is formed between the source electrode 12 and the drain electrode 13. Rather, the semiconductor layer 21 is formed on top of the semiconductor layer 16, without contacting any source electrodes or drain electrodes (see Dodabalapur et al., col. 5, lines 6-13 and Fig. 2).

Moreover, Dodabalapur et al. discuss the semiconductor layer 21 being in direct contact with the semiconductor layer 16, which is of the opposite conductivity type as layer 21, to form a p-n junction (see Dodabalapur et al., col. 5, lines 6-13, and Fig. 2). This p-n junction configuration is completely distinct from the configuration of the field effect transistor as required by claim 20.

In addition, the present record fails to provide any motivation necessary for combining the references to require the following steps in the order of 1) forming a p-type semiconductor layer between the source electrode and the drain electrode so as to form a plurality of p-type field effect transistors on the substrate, and then 2) selectively converting some of the p-type field effect transistors into an n-type by dispensing an n-type modifying polymer layer on the p-type semiconductor layer, as required by claim 20. Shim et al. discuss a method of converting a p-type carbon nanotube into an n-type. Bai et al. discuss depositing polymers by ink jet dispensing method. However, nowhere in Dodabalapur et al., Shim et al. or Bai et al. teaches or suggests performing the above steps in the order as required by claim 20. The teachings in the reference disclosures in no way suggests that advantages such as simplifying the process for manufacturing an electrical element array including p-type and n-type carbon nanotube field effect transistors on the same substrate by the present method can be obtained.

For at least these reasons above, claim 20 is patentable over Dodabalapur et al. in view of Shim et al., and further in view of Bai et al.

In view of the above, favorable reconsideration in the form of a notice of allowance is respectfully requested. Any questions regarding this communication can be directed to the undersigned attorney, Douglas P. Mueller, Reg. No. 30,300, at (612) 455-3804.

Respectfully submitted,

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